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4	US 20040060023 A1	20040325	25	Voltage island chip implementation	716/7
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23	US 6523150 B1	20030218	17	Method of designing a voltage partitioned wirebond package	716/4
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29	US 4757416 A	19880712	26	Protective apparatus, methods of operating same and phase window adjusting apparatus for use therein	361/84
30	US 4295149 A	19811013	<u>*</u>	Master image chip organization technique or method	257/211
177 1	US 3881175 A	19750429	•	Integrated circuit SOS memory subsystem and method of making same	365/176

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